ISOLATED 3.3-V FULL AND HALF-DUPLEX RS-485 TRANSCEIVERS

FEATURES

- **4000-V_{PEAK} Isolation, 560-Vpeak V_{IORM} UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2)**
- **1/8 Unit Load – Up to 256 Nodes on a Bus**
- **Meets or Exceeds TIA/EIA RS-485 Requirements**
- **Signaling Rates up to 1 Mbps**
- **Thermal Shutdown Protection**
- **Low Bus Capacitance – 16 pF (Typ)**
- **50 kV/μs Typical Transient Immunity**
- **Fail-safe Receiver for Bus Open, Short, Idle**
- **3.3-V Inputs are 5-V Tolerant**

APPLICATIONS

- **Security Systems**
- **Chemical Production**
- **Factory Automation**
- **Motor/motion Control**
- **HVAC and Building Automation Networks**
- **Networked Security Stations**

DESCRIPTION

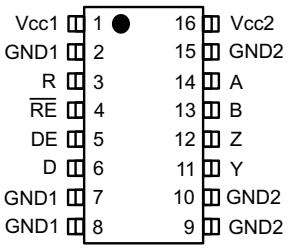
The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications.

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 Vrms of isolation for 60s between the bus-line transceiver and the logic-level interface.

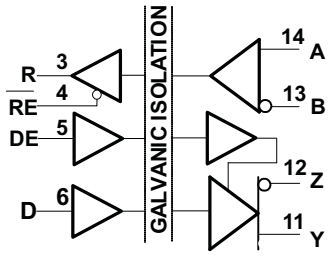
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The ISO15 and ISO35 are qualified for use from –40°C to 85°C.

DW PACKAGE



function diagram



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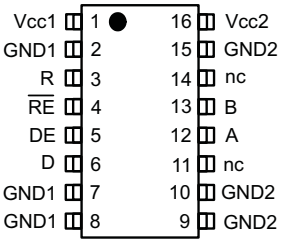
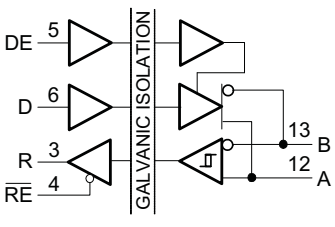


function diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Input supply voltage. (2) V_{CC1}, V_{CC2}				–0.3 to 6	V
V_O	Voltage at any bus I/O terminal				–9 to 14	V
V_{IT}	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 11)				–50 to 50	V
V_I	Voltage input at any D, DE or $\overline{RE}$ terminal				–0.5 to 7	V
I_O	Receiver output current				±10	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus pins and GND1	±6	kV
				Bus pins and GND2	±16	
				All pins	±4	
		Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1	kV
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage, V_{CC1}, V_{CC2}		3.15	3.3	3.6	V
V_{OC}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
R_L	Differential input resistance		54	60		Ω
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
T_J	Operating junction temperature		–40		150	°C

SUPPLY CURRENT

over recommended operating condition (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Logic-side supply current	ISO35	$\overline{RE}$ at 0 V or Vcc, DE at 0 V, No load (driver disabled)			8	mA
			$\overline{RE}$ at 0 V or Vcc, DE at V_{CC}, No Load (driver enabled)			8	
		ISO15	$\overline{RE}$ at 0 V or Vcc, DE at 0 V, No load (driver disabled)			8	mA
			$\overline{RE}$ at 0 V or Vcc, DE at V_{CC}, No Load (driver enabled)			8	
I_{CC2}	Bus-side supply current	ISO35	$\overline{RE}$ at 0 V or Vcc, DE at 0 V, No load (driver disabled)			15	mA
			$\overline{RE}$ at 0 V or Vcc, DE at V_{CC}, No Load (driver enabled)			19	
		ISO15	$\overline{RE}$ at 0 V or Vcc, DE at 0 V, No load (driver disabled)			15	mA
			$\overline{RE}$ at 0 V or Vcc, DE at V_{CC}, No Load (driver enabled)			19	

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	I_O = 0 mA, no load			2.5		V_{CC}	V
		R_L = 54 Ω, See Figure 1			1.5	2		
		R_L = 100 Ω (RS-422), See Figure 1			2	2.3		
		V_{test} from –7 V to +12 V, See Figure 2			1.5			
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of the differential output voltage	See Figure 1 and Figure 2			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3			1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.1		0.1	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 3				0.5		V
I_I	Input current	D, DE, V_I at 0 V or V_{CC1}			–10		10	µA
I_{OZ}	High-impedance state output current	ISO15	See receiver input current					
		IDO35	V_Y or V_Z = 12 V	Other input at 0 V			90	µA
			V_Y or V_Z = 12 V, V_{CC} = 0		–10			
			V_Y or V_Z = –7 V				90	
			V_Y or V_Z = –7 V, V_{CC} = 0		–10			
I_{OS}	Short-circuit output current	V_A or V_B at –7 V		Other input at 0 V	–250		250	mA
		V_A or V_B at 12 V						
$C_{(OD)}$	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V				16		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 12 and Figure 13			25	50		kV/µs

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 4			340	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			6		
t_r	Differential output signal rise time		120	185	300	
t_f	Differential output signal fall time	See Figure 5	120	180	300	ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output				205	µs
t_{PZH}	Propagation delay, high-impedance-to-high-level output	See Figure 6			530	µs
t_{PLZ}	Propagation delay, low-level to high-impedance output				330	
t_{PZL}	Propagation delay, standby-to-low-level output				530	

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	I_O = –8 mA				–20	mV
$V_{IT(–)}$	Negative-going input threshold voltage	I_O = 8 mA		–200			mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				50		mV
V_O	Output voltage	V_{ID} = 200 mV, See Figure 7	I_O = –8 mA	2.4			V
			I_O = 8 mA			0.4	
$I_{O(Z)}$	High-impedance state output current	V_I = –7 to 12 V, Other input = 0 V		–1		1	µA
I_A or I_B	Bus input current	V_A or V_B = 12 V	Other input at 0 V		0.05	0.1	mA
		V_A or V_B = 12 V, V_{CC} = 0			0.05	0.1	
		V_A or V_B = –7 V		–0.1	–0.04		
		V_A or V_B = –7 V, V_{CC} = 0		–0.1	–0.03		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		–10			µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V		–10			µA
R_{ID}	Differential input resistance	A, B		48			kΩ
C_D	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5V, DE at 0 V			16		pF

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO15	See Figure 8			100	ns
		ISO35				100	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$)	ISO15				13	ns
		ISO35				13	
t_r	Output signal rise time				2	4	ns
t_f	Output signal fall time				2	4	
t_{PZH}, t_{PZL}	Propagation delay, high-impedance-to-high-level output Propagation delay, standby-to-low-level output		DE at 0 V, See Figure 9 and Figure 10		13	25	ns
t_{PHZ}, t_{PLZ}	Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output				13	25	ns

PARAMETER MEASUREMENT INFORMATION

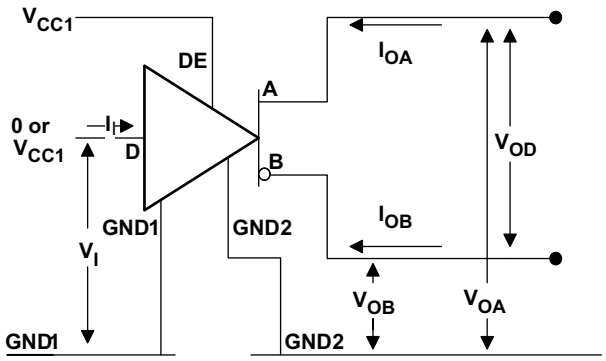


Figure 1. Driver V_{OD} Test and Current Definitions

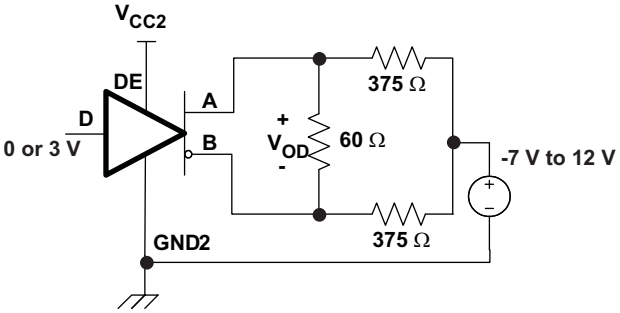
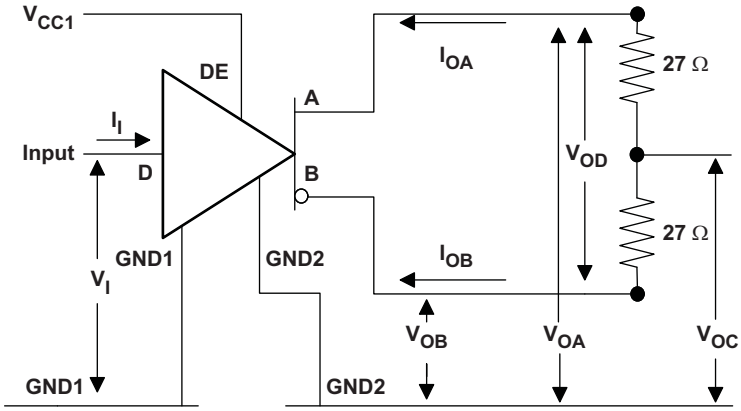


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



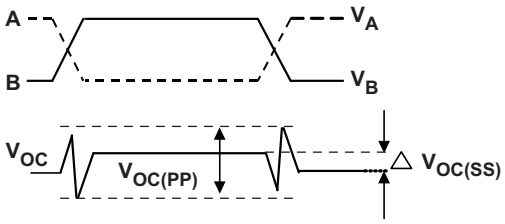
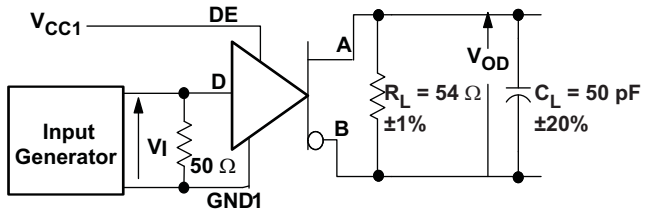
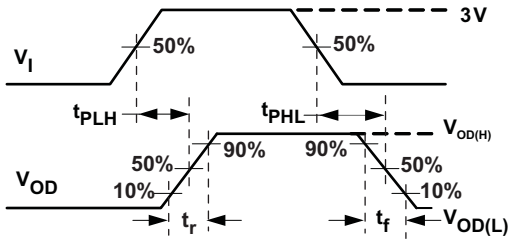


Figure 3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage





Generator: PRR = 500 kHz, 50% duty cycle, t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and Instrumentation Capacitance

Figure 4. Driver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

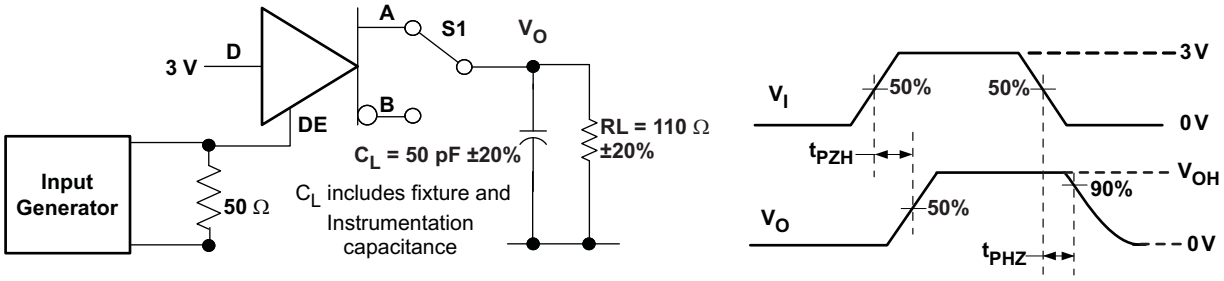
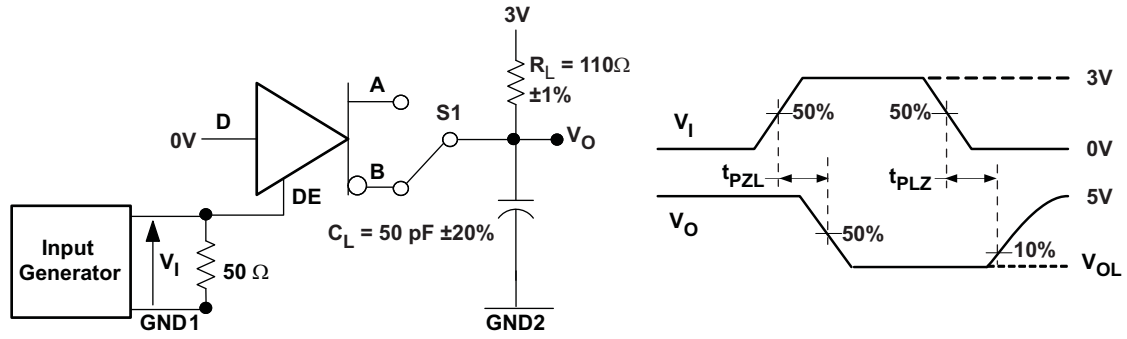


Figure 5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% duty cycle,
t_r <6ns, t_f <6ns, Z_O = 50Ω

C_L includes fixture and
Instrumentation capacitance

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

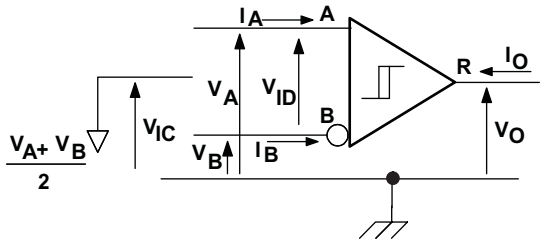
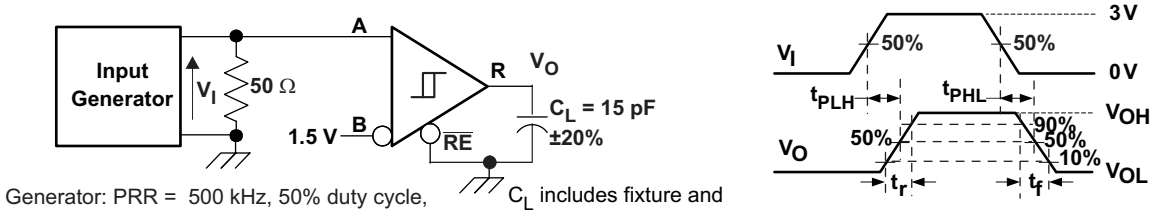


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% duty cycle,
t_r <6ns, t_f <6ns, Z_O = 50 Ω

C_L includes fixture and
instrumentation capacitance

Figure 8. Receiver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

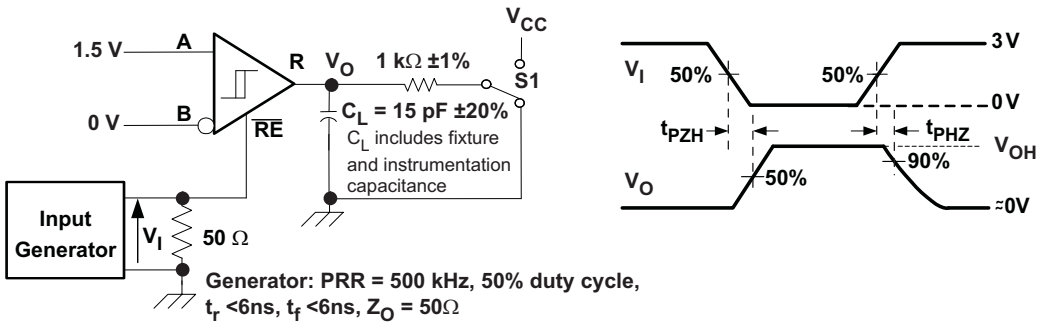


Figure 9. Receiver Enable Test Circuit and Waveforms, Data Output High

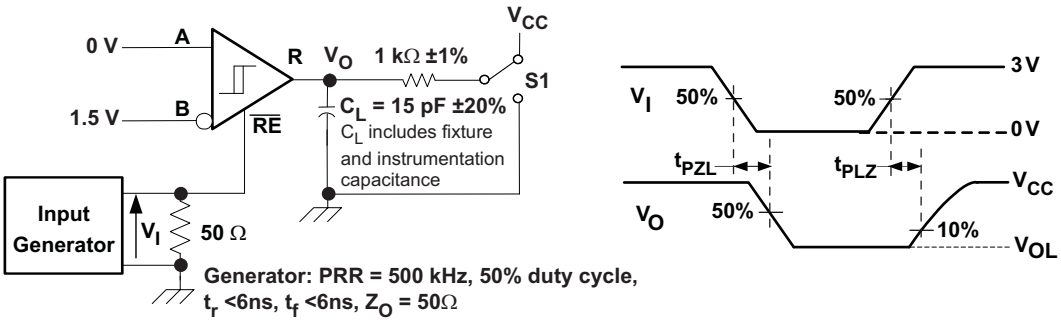
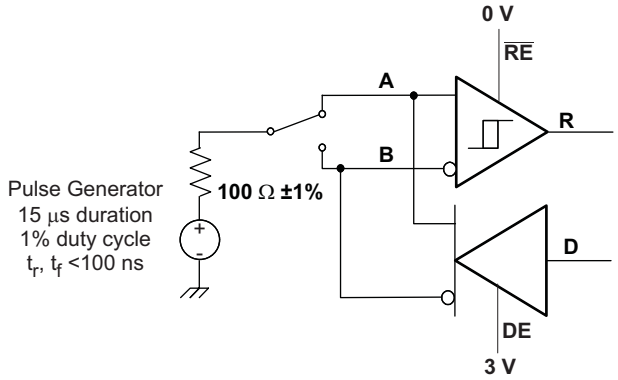


Figure 10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.
Data stability at the R output is not specified.

Figure 11. Transient Over-Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

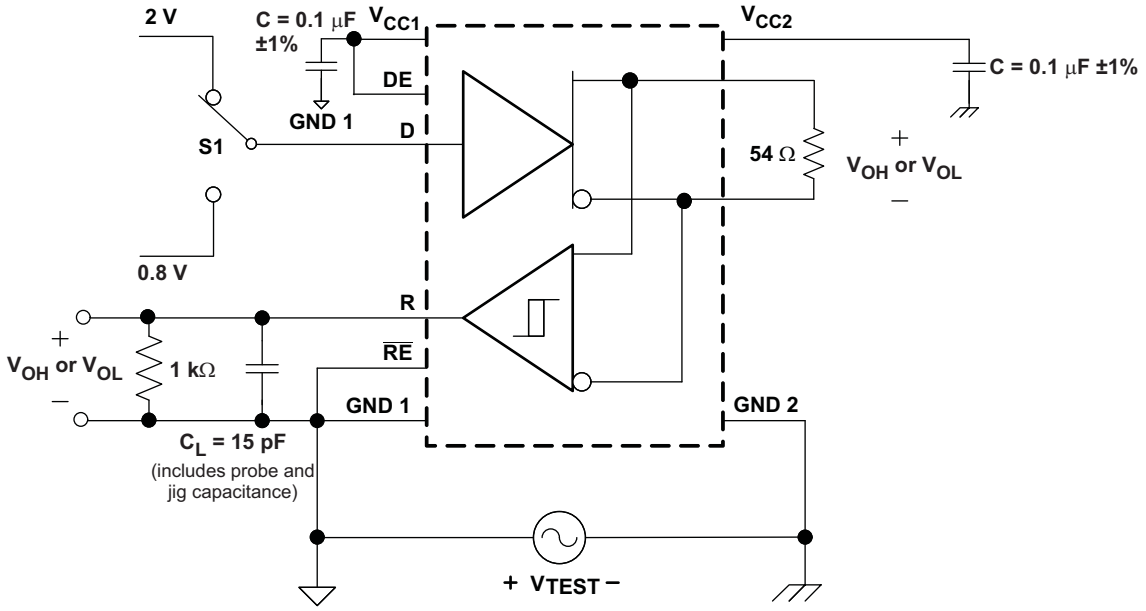


Figure 12. Half-Duplex Common-Mode Transient Immunity Test Circuit

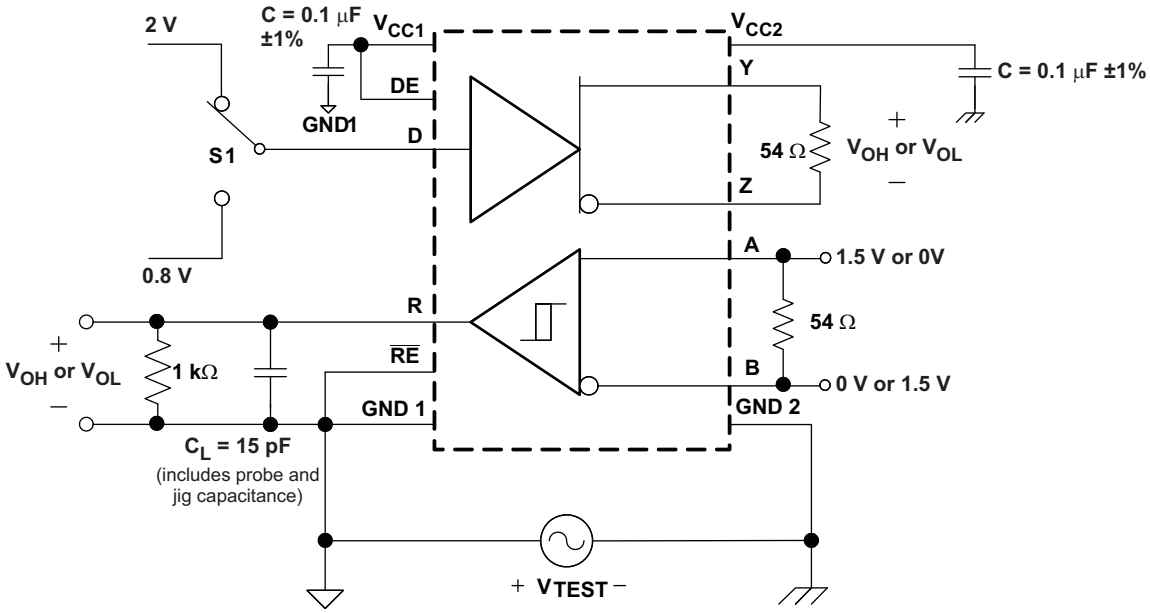


Figure 13. Full-Duplex Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

Table 1. Driver Function Table

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS	
				A or Y	B or Z
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

Table 2. Receiver Function Table

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$-0.01\ V \le V_{ID}$	L	H
PU	PU	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	$V_{ID} \le -0.2\ V$	L	L
PU	PU	X	H	Z
PU	PU	X	OPEN	Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Z
PU	PD	X	L	H

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III
	Rated mains voltage ≤ 400 V_{RMS}	I-II

IEC 60747-5-2 INSULATION CHARACTERISTICS (1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Clasification 40/125/21

REGULATORY INFORMATION

VDE	UL
Certified according to IEC 60747-5-2	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: E181974

(1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			210	mA
T_S	Maximum case temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-Air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 20 MHz 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric defintions of EIA/JESD51-3 for leaded surface mount packages.

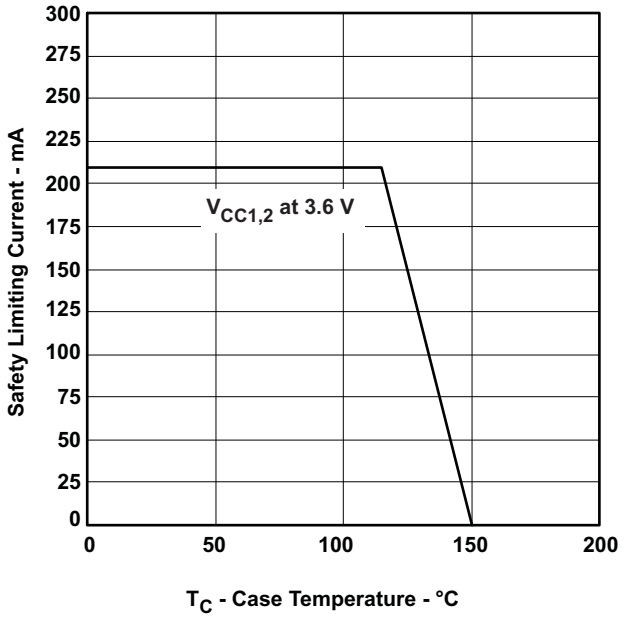
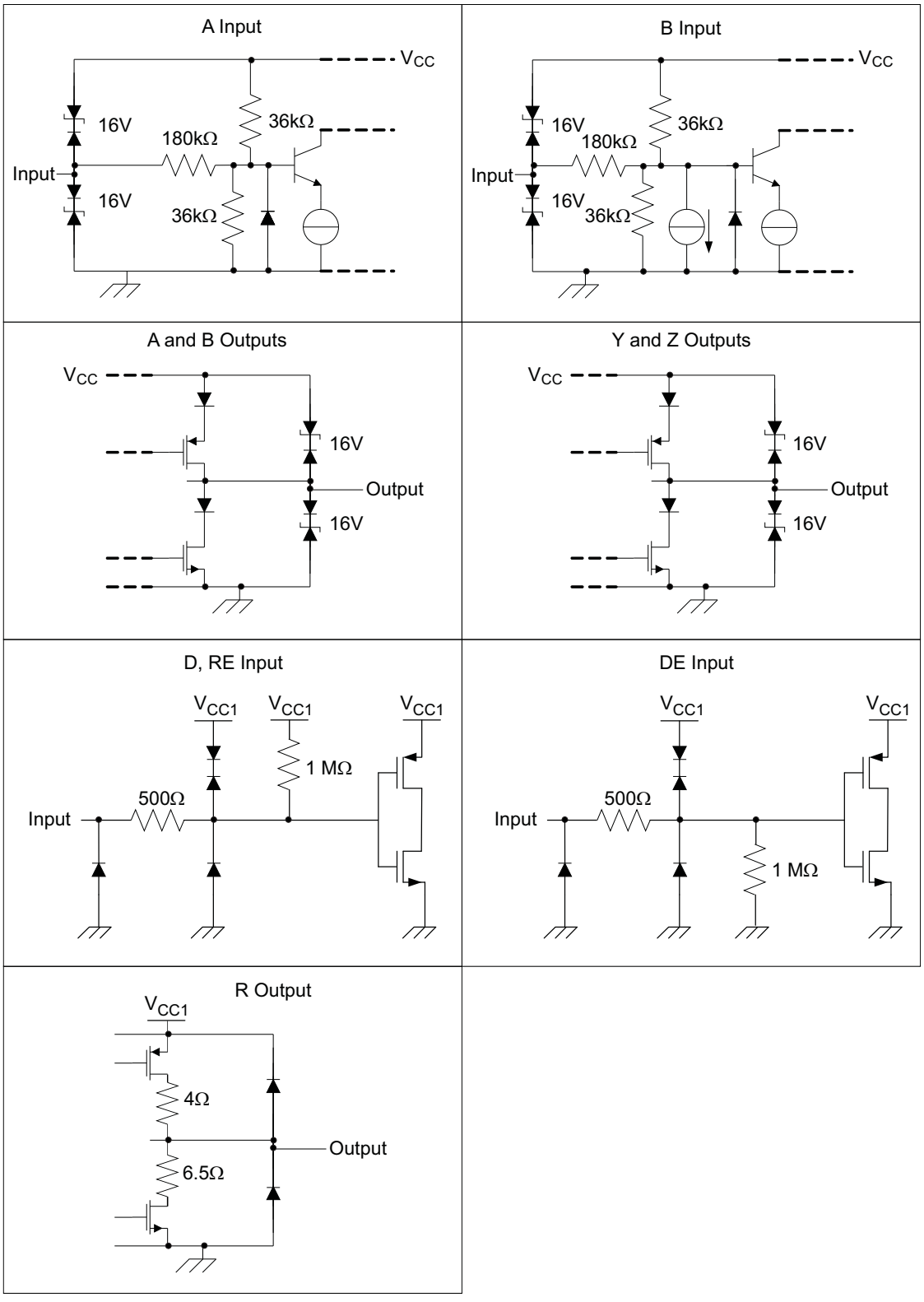


Figure 14. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

EQUIVALENT CIRCUIT SCHEMATICS



TYPICAL CHARACTERISTICS CURVES

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

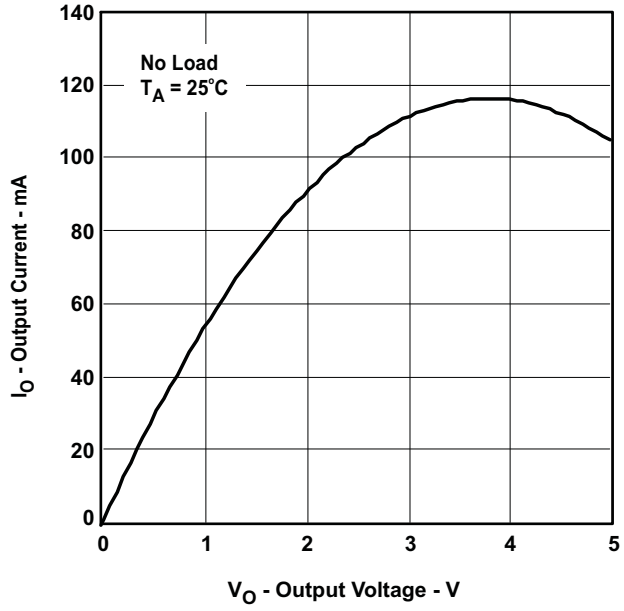


Figure 15.

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

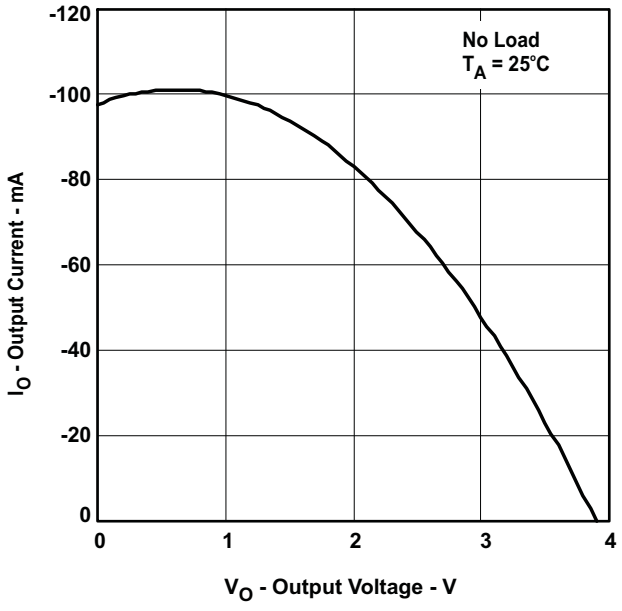


Figure 16.

RMS SUPPLY CURRENT
vs
SIGNALING RATE

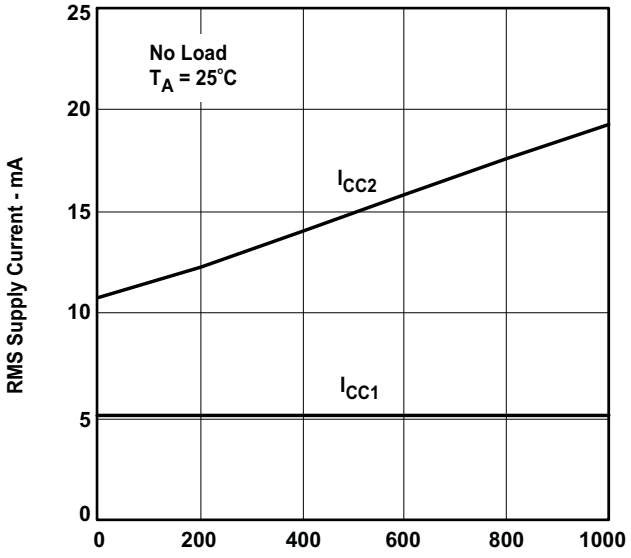


Figure 17.

BUS INPUT CURRENT
vs
INPUT VOLTAGE

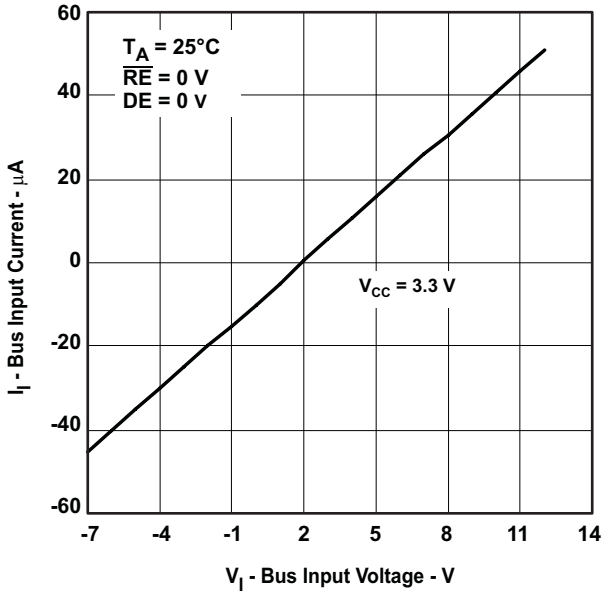


Figure 18.

TYPICAL CHARACTERISTICS CURVES (continued)

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

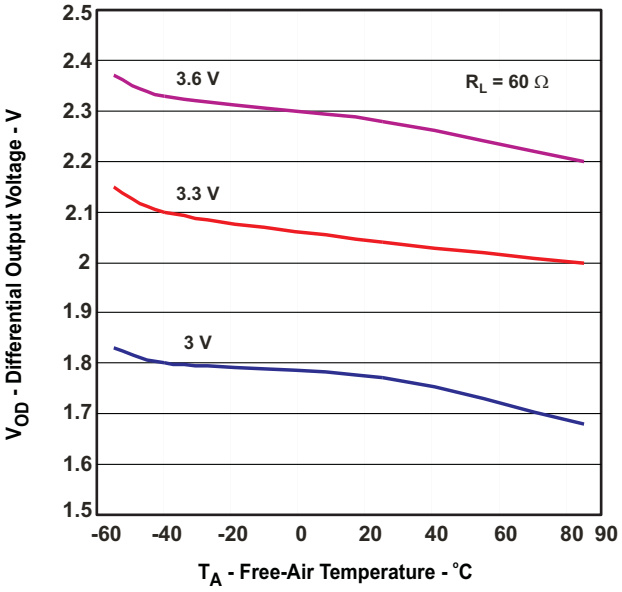


Figure 19.

DRIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

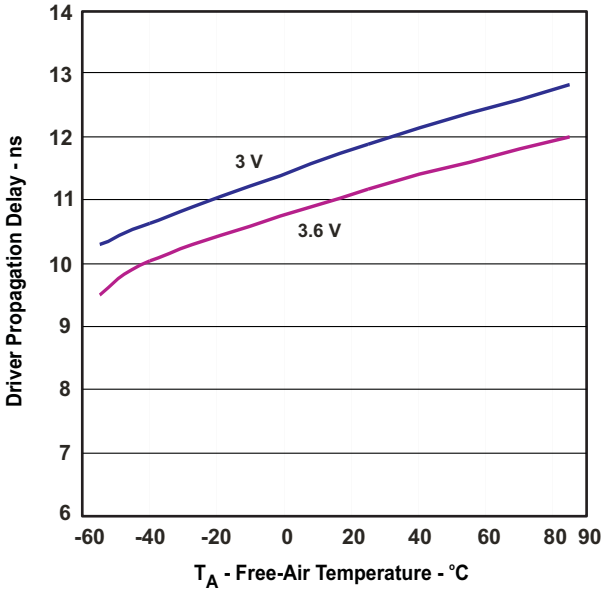


Figure 20.

APPLICATION INFORMATION

Transient Voltages

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation. The transient ratings of the ISO15 and ISO35 are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment, and can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high voltage transients.

Figure 21 models the ISO15 and ISO35 bus IO connected to a noise generator. C_{IN} and R_{IN} is capacitance or resistance across the device and any other stray or added capacitance or resistance across the A or B pin to GND2. C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of the ISO15 and ISO35 plus those of any other insulation (transformer, etc.). The stray inductance is assumed to be negligible. From this model, the voltage at the isolated bus return is,

$$V_{GND2} = V_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \quad (1)$$

and will always be less than 16 V from V_N. If the ISO15 and ISO35 are tested as a stand-alone device, R_{IN} = 6 ɹ$10^4\Omega$, C_{IN} = 16 ɹ10^{-12} F, R_{ISO} = $10^9\Omega$ and C_{ISO} = 10^{-12} F.

Note from Figure 21 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency,

$$\frac{V_{GND2}}{V_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6x10^4} \quad (2)$$

or essentially all of noise appears across the barrier. At high frequency,

$$\frac{V_{GND2}}{V_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94 \quad (3)$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier.

It is not recommend for the user to test equipment transient susceptibility with ESD generators, or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

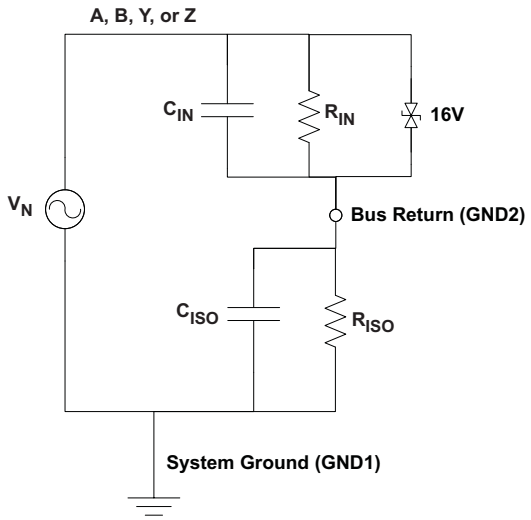


Figure 21. Noise Model

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO15DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO15DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO15DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO15DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO35DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO35DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO35DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ISO35DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

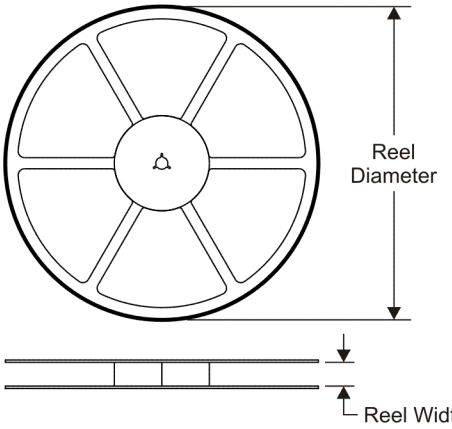
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

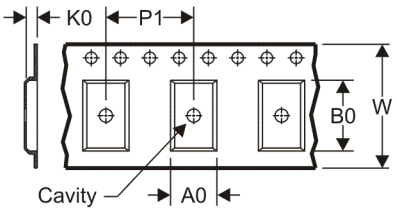
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

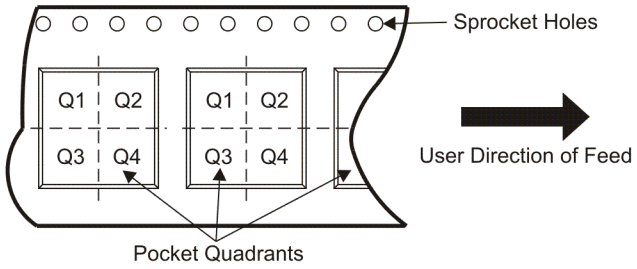


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

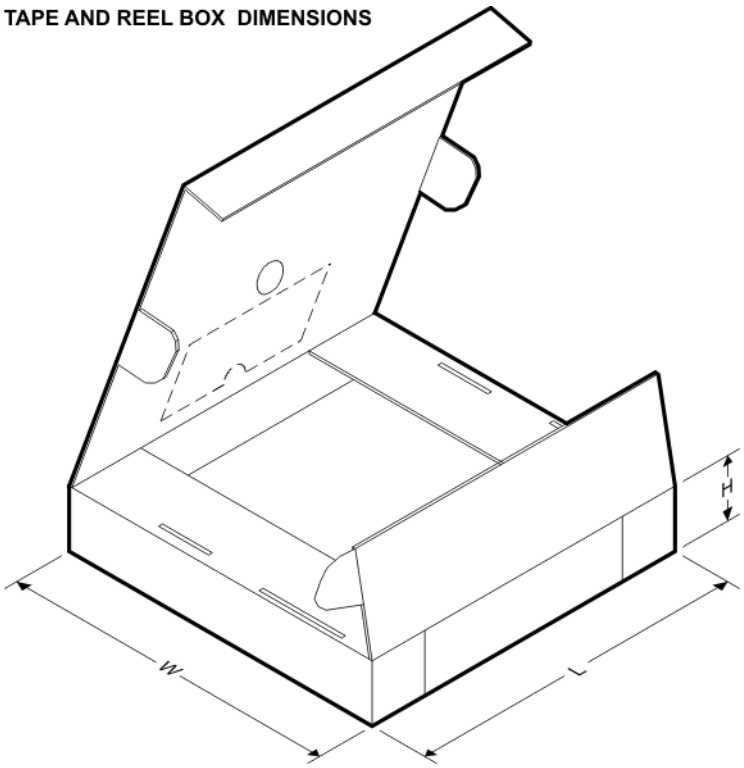
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO15DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

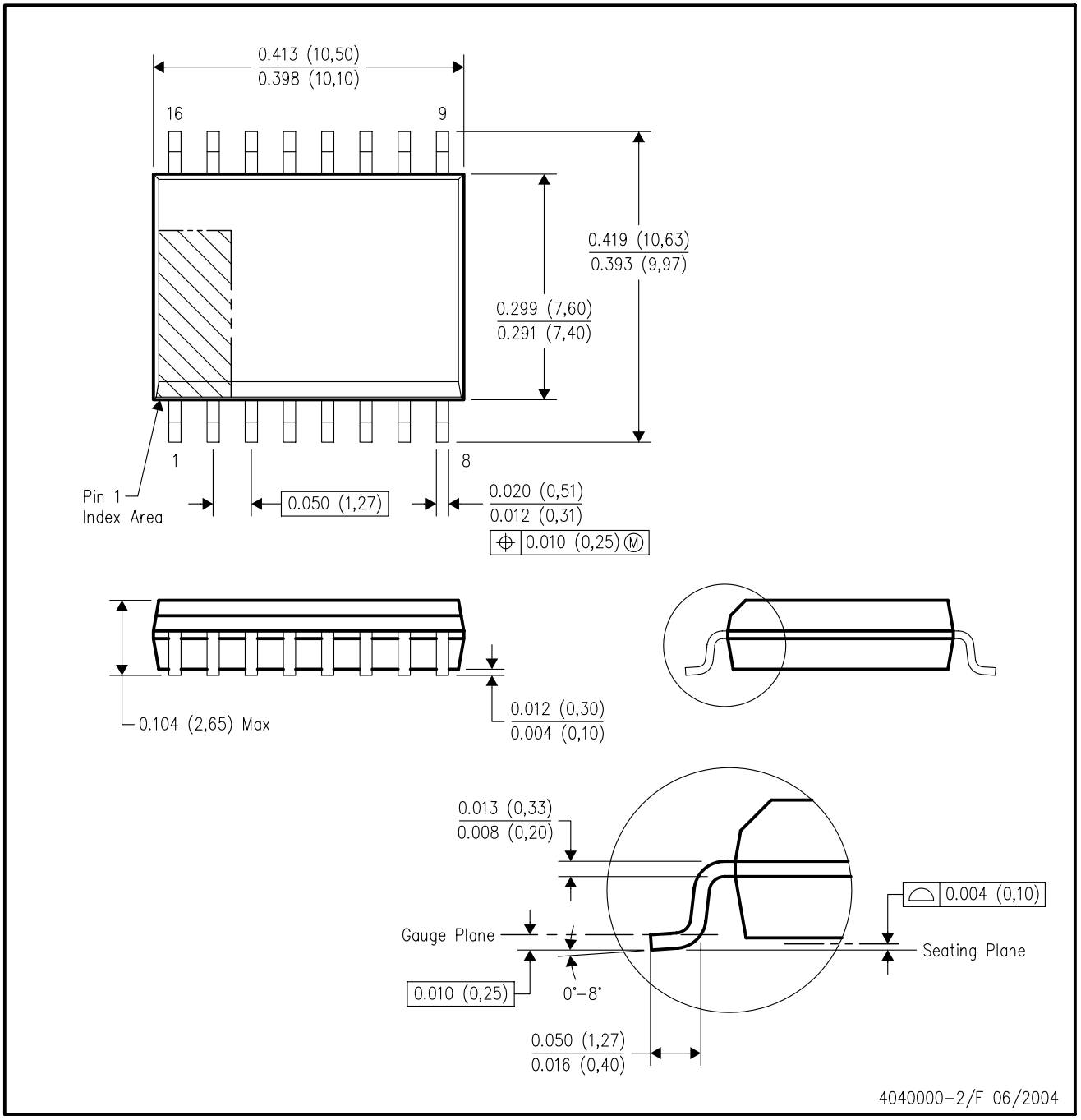
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO15DWR	SOIC	DW	16	2000	358.0	335.0	35.0
ISO35DWR	SOIC	DW	16	2000	358.0	335.0	35.0

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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